

WHAT IS CLAIMED IS:

1           1. In a processor with an n-way associative cache,  
2 a method for prefetching data to the cache comprising the  
3 steps of:

4           issuing a prefetch instruction, wherein said  
5 prefetch instruction includes a hint field and address  
6 information;

7           addressing the cache using said address information  
8 contained in said prefetch instruction;

9           indicating a cache miss for said data addressed by  
10 said prefetch instruction;

11           specifying a refill destination for said data in a  
12 first portion of said hint field, wherein said destination is  
13 a first way in said cache; and  
14           refilling said cache.

1           2. The method of claim 1 further comprising the  
2 step of enabling said specifying step using a second portion  
3 of said hint field.

1           3. The method of claim 2 wherein said refilling  
2 step refills said first way of said cache.

1           4. The method of claim 1 further comprising the  
2 step of disabling said specifying step using a second portion  
3 of said hint field.

1           5. The method of claim 4 further comprising the  
2 step of refilling a second way of said cache based on a least-  
3 recently-used protocol.

1           6. A processor comprising:  
2           a decoder for decoding a prefetch instruction,  
3 wherein said prefetch instruction includes a hint field and  
4 address information;  
5           a first n-way set-associative cache, coupled to said  
6 decoder, containing a first-cache line that is addressed using  
7 said address information;

8 a first comparator means, coupled to said first  
9 cache, for indicating a first-cache miss when said first-cache  
10 line is addressed and does not contain desired data; and

11 a first selection means, coupled to said first  
12 cache, for choosing a destination indicator for refilling said  
13 first-cache line with said desired data based on a first  
14 portion of said hint field.

1 7. The processor of claim 6 wherein said  
2 destination indicator is a second portion of said hint field.

1 8. The processor of claim 6 wherein said  
2 destination indicator is an LRU bit.

1 9. The processor of claim 7 wherein said second  
2 portion of said hint field points to a first way of said first  
3 cache, wherein said first way contains streamed data.

1 10. The processor of claim 7 wherein said second  
2 portion of said hint field points to a second way of said  
3 first cache, wherein said second way contains retained data.

1 11. The processor of claim 9 further comprising a  
2 means for disabling a refill operation of said cache line when  
3 said first way is unavailable.

1 12. The processor of claim 6 further comprising:  
2 a second n-way set-associative cache, coupled to  
3 said first cache, containing a second cache line that is  
4 addressed using said address information;

5 a second comparator means, coupled to said second  
6 cache, for indicating a second-cache miss when said second  
7 cache line is addressed; and

8 a second selection means, coupled to said second  
9 cache, for choosing said destination indicator for refilling  
10 said second cache line based on said first portion of said  
11 hint field.

1 13. A processor comprising:

2 a decoder for decoding a prefetch instruction, said  
3 prefetch instruction including a hint field and being used to  
4 refill desired data to a first n-way associative cache; and

5 a first multiplexer, coupled to said decoder, for  
6 choosing a destination indicator based on a first portion of  
7 said hint field, said destination indicator being used to  
8 direct refilling of said first cache with said desired data.

1 14. The processor of claim 13 wherein said  
2 destination indicator is a second portion of said hint field.

1 15. The processor of claim 13 wherein said  
2 destination indicator is an LRU bit.

1 16. The processor of claim 14 wherein said second  
2 portion of said hint field points to a first way of said first  
3 cache, wherein said first way contains streamed data.

1 17. The processor of claim 14 wherein said second  
2 portion of said hint field points to a second way of said  
3 first cache, wherein said second way contains retained data.

1 18. The processor of claim 13 further comprising:  
2 a second multiplexer, coupled to said decoder, for  
3 choosing said destination indicator based on said first  
4 portion of said hint field, said destination indicator being  
5 used to direct refilling of a second cache with said desired  
6 data.

1 19. The processor of claim 13 wherein said  
2 destination indicator is a randomly generated bit.

Add  
BI